Notice of Allowability	Application No.	Applicant(s)	
	10/801,993	MOULI, CHANDRA V.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-31 and 38-44*.

3. ☒ The drawings filed on *16 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3/16/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Adeel Akhtoar on 11/24/04.

The application has been amended as follows:

Claims 32-37 have been canceled.

Allowable Subject Matter

2. Claims 1-31 and 38-44 are allowed.

3. The following is an examiner's statement of reasons for allowance:

In claim 1, the patentability, at least in part, is a combination of: "*a method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (BOX) layer and an active layer above the BOX layer, the method comprising: forming gate stacks on the device regions so as to define underlying channel regions; forming a masking layer with openings at least partially over the gate stacks and so as to mask remaining regions of the SOI structure not underlying the gate stacks;* ***implanting first additional dopants through the openings such that the additional dopants come to reside within the BOX layer underlying the channel regions so as to create localized borophosphosilicate glass (BPSG) diffusion***

sources within the BOX layer; *implanting second threshold adjust dopants into the n-wells and p-wells to change a threshold voltage of the resulting transistor devices; and processing the SOI structure so as to induce the diffusion sources to establish retrograde dopant profiles in the channel regions having a peak concentration near the BOX".*

In claim 11, the patentability, at least in part, is a combination of: "*a method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (BOX) layer and an active layer above the BOX layer, the method comprising: forming gate stacks on the device regions so as to define underlying channel regions; forming a masking layer with asymmetric openings at least partially over the gate stacks and so as to mask remaining regions of the SOI structure not underlying the gate stacks;* ***implanting first additional dopants through the openings such that the additional dopants come to reside within the BOX layer underlying the channel regions so as to create asymmetric borophosphosilicate glass (BPSG) diffusion sources within the BOX layer****; and processing the SOI structure so as to induce the diffusion sources to establish retrograde dopant profiles in the channel regions having a peak concentration near the BOX".*

In claim 21, the patentability, at least in part, is a combination of: "*a method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (BOX) layer and an active layer above the BOX layer, the method comprising: forming gate stacks on the device regions so as to define underlying channel regions; forming a masking layer with openings at least partially over the gate stacks and so as to mask remaining regions of the SOI structure not overlying the gate stacks;* ***implanting first additional dopants through the openings such that the additional dopants come to reside within the BOX layer underlying the***

***channel regions so as to create borophosphosilicate glass (BPSG) diffusion sources within the BOX layer**; and processing the SO1 structure so as to induce the diffusion sources to establish retrograde dopant profiles in the channel regions having a peak concentration near the BOX".*

In claim 38, the patentability, at least in part, is a combination of: "*a method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (B0X) layer and an active layer above the BOX layer, the method comprising: forming gate stacks on the device regions so as to define underlying channel regions; **implanting first additional dopants through the gate stacks such that the additional dopants come to reside within the BOX layer underlying the channel regions and substantially between the source and drain regions so as to create borophosphosilicate glass (BPSG) diffusion sources within the BOX layer**; and processing the SO1 structure so as to induce the diffusion sources to establish retrograde dopant profiles in the channel regions having a peak concentration near the BOX".*

4. The art of record (including the record of IDS filed on 03/16/04) does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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